

REMARKS

We have canceled independent claims 1 and 11 and have amended dependent claims 2 and 12 to be in independent form and to include all of the features recited in claims 1 and 11 respectively.

Prior Art Rejections

Claims 1-6 and 11-12 were rejected under 35 U.S.C. 102(e) as being anticipated by Minamino et al. (hereafter Minamino)(US 6,657,929). As noted above, we have amended claims 2 and 12 to include all of the features recited in independent claims 1 and 11, respectively. Applicant traverses this rejection.

We submit that Minamino does not disclose a hold signal generator for generating a first hold signal that holds the frequency of the oscillation signal of the PLL circuit during a first period in accordance with the detection, and a second hold signal that holds the frequency of the oscillation signal of the PLL circuit during a second period in accordance with the detection, which differs from the first period as, recited in amended claim 2. We further submit that Minamino does not disclose a monitor that generates a first hold signal that holds the frequency of the oscillation signal of the PLL circuit during a first period between a first timing and a second timing, at which the cycle of the wobble signal changes, and a second hold signal that holds the frequency of the oscillation signal of the PLL circuit during a second period, which is longer than the first period of the first hold signal measured from the first timing, as recited in amended claim 12.

Rather, Minamino (USPN 6,657,929) discloses the first wobble failure detection circuit 72 that generates a high-level wobble PLL hold signal when the count of the output clock from the wobble PLL circuit 14 exceeds a threshold L1 corresponding to the time period t1 during which the wobble signal fails, and the second wobble failure detection circuit 73 that generates a wobble usable 3 signal via the inverter when the count value exceeds a threshold L2 corresponding to the time period t2 during which the wobble signal fails (see column 17, lines 10-53 of Minamino). That is, the second wobble failure detection circuit 73 of Minamino generates the wobble usable 3 signal for

Applicant(s) : Hideki Hirayama et al.
Serial No. : 10/781,330
Filed : February 18, 2004
Page : 7 of 8

Attorney Docket No.: 35901-079001
Client Ref. No.: P1S2003324US

allowing the usage of the wobble signal when the period of the count of the output clock from the wobble PLL circuit 14 (the period of a low level output from the wobble digitizing circuit 13) is shorter than the time period t_2 . Accordingly, the second wobble failure detection circuit 73 of Minamino does not generate a hold signal that holds the frequency of the oscillation signal of the PLL circuit. Accordingly, the invention of claims 2-6 and 12 distinguishes over Minamino.

Claims 7-10 and 13 were rejected under 35 U.S.C. 103(a) as being unpatentable over Minamino in view of Katoh (US 6,088,311). Applicant traverses this rejection.

We believe that neither Minamino nor Katoh disclose the above feature of the present invention. Accordingly, we believe that the present invention of claims 7-10 and 13 is not obvious over Minamino in view of Katoh.

Conclusion

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

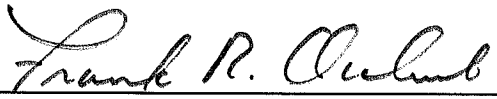
The request for examination fee in the amount of \$790 is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to Deposit Account No. 50-4189, referencing Attorney Docket No. 35901-079001.

Applicant(s) : Hideki Hirayama et al.
Serial No. : 10/781,330
Filed : February 18, 2004
Page : 8 of 8

Attorney Docket No.: 35901-079001
Client Ref. No.: P1S2003324US

Respectfully submitted,

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